

Abstract of the Disclosure

A source region and a drain region are formed on the surface of a silicon substrate, and a gate insulating film and a gate electrode are formed in this order on a channel
5 region between the source region and the drain region. An interlayer insulating film is formed on the silicon substrate so as to cover the gate electrode and the gate insulating film, and a contact hole is formed in the interlayer insulating film on the gate electrode. A connecting layer
10 and a lower electrode composed of $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ are formed in the contact hole. A ferroelectric film composed of $\text{SrBi}_2\text{Ta}_2\text{O}_9$, and an upper electrode composed of $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ are formed in this order on the interlayer insulating film so as to be brought into contact with the upper surface of the lower electrode.